

FIG. 1 is a schematic diagram of a prior art device 100. The device 100 includes a substrate 102, a gate stack 104, a gate electrode 106, a channel layer 108, a source/drain region 110, a source/drain electrode 112, a source/drain contact 114, a source/drain pad 116, a source/drain pad 118, a source/drain pad 120, a source/drain pad 122, a source/drain pad 124, a source/drain pad 126, a source/drain pad 128, a source/drain pad 130, a source/drain pad 132, a source/drain pad 134, a source/drain pad 136, a source/drain pad 138, a source/drain pad 140, a source/drain pad 142, a source/drain pad 144, a source/drain pad 146, a source/drain pad 148, a source/drain pad 150.

**Fig. 1**  
(Prior Art)

100

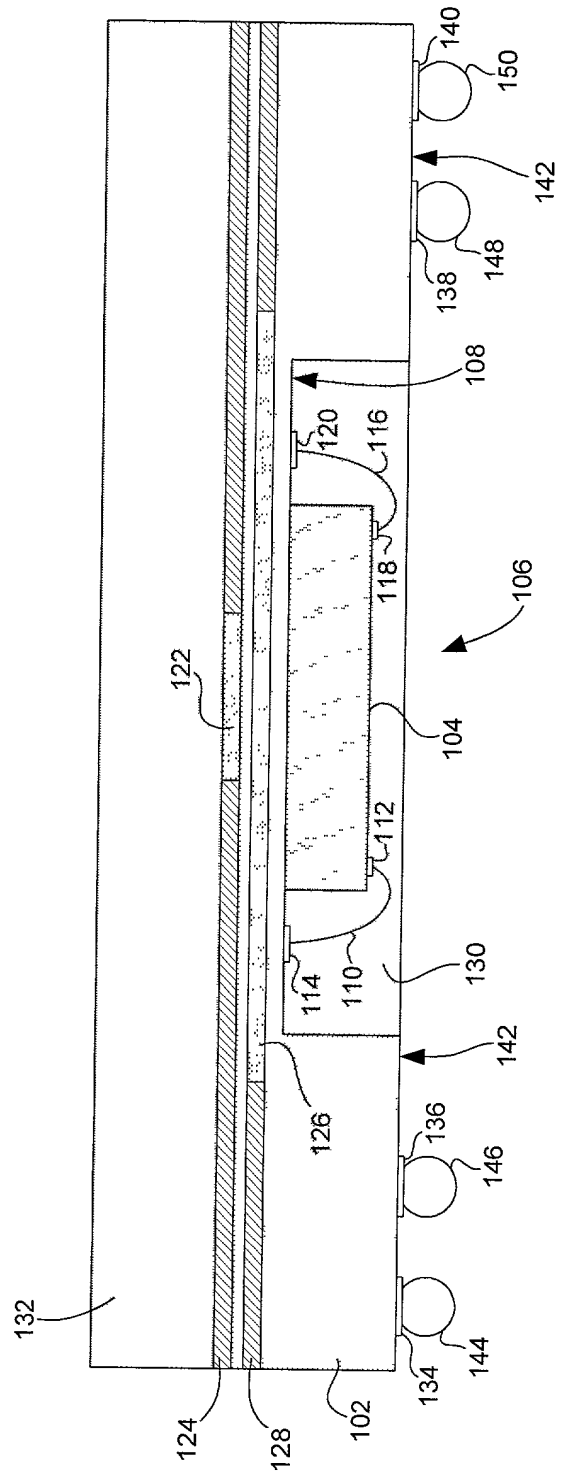
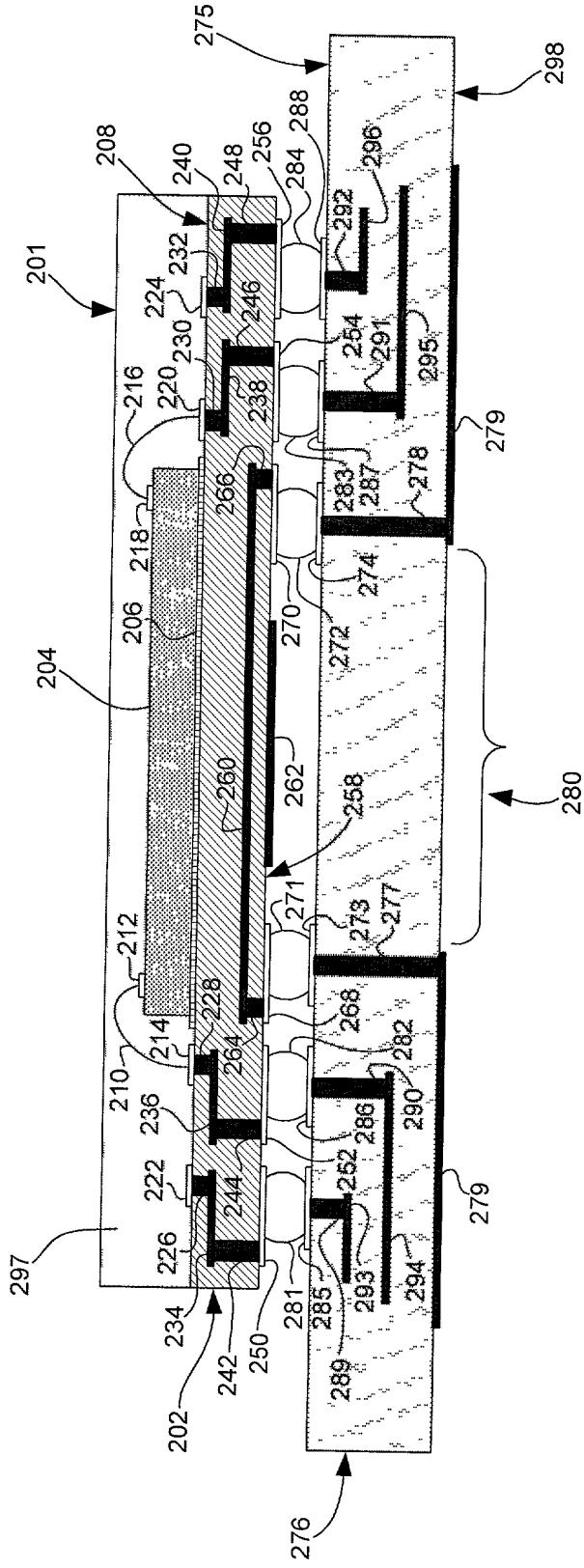


Fig. 2

FIG. 2 is a cross-sectional view of a semiconductor device 200, showing a substrate 202, a gate stack 204, and a channel layer 206. The device includes a source region 208, a drain region 210, and a gate electrode 212. The channel layer 206 is disposed between the source and drain regions. The gate stack 204 is disposed on top of the channel layer 206. The device is shown in a cross-sectional view along a line A-A.

200



**Fig. 3**

